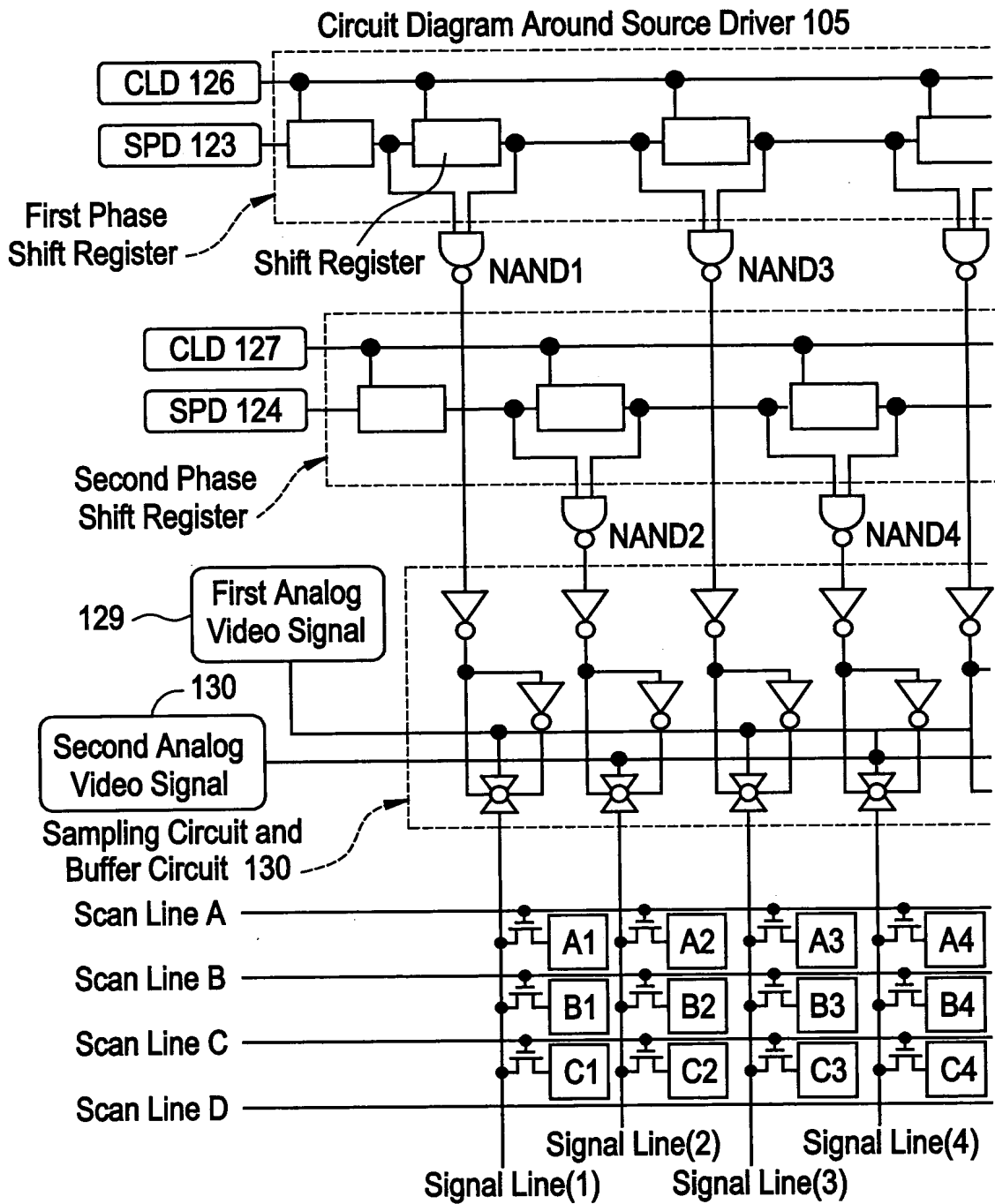


FIG. 2A**FIG. 2B****Display Pattern**

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4

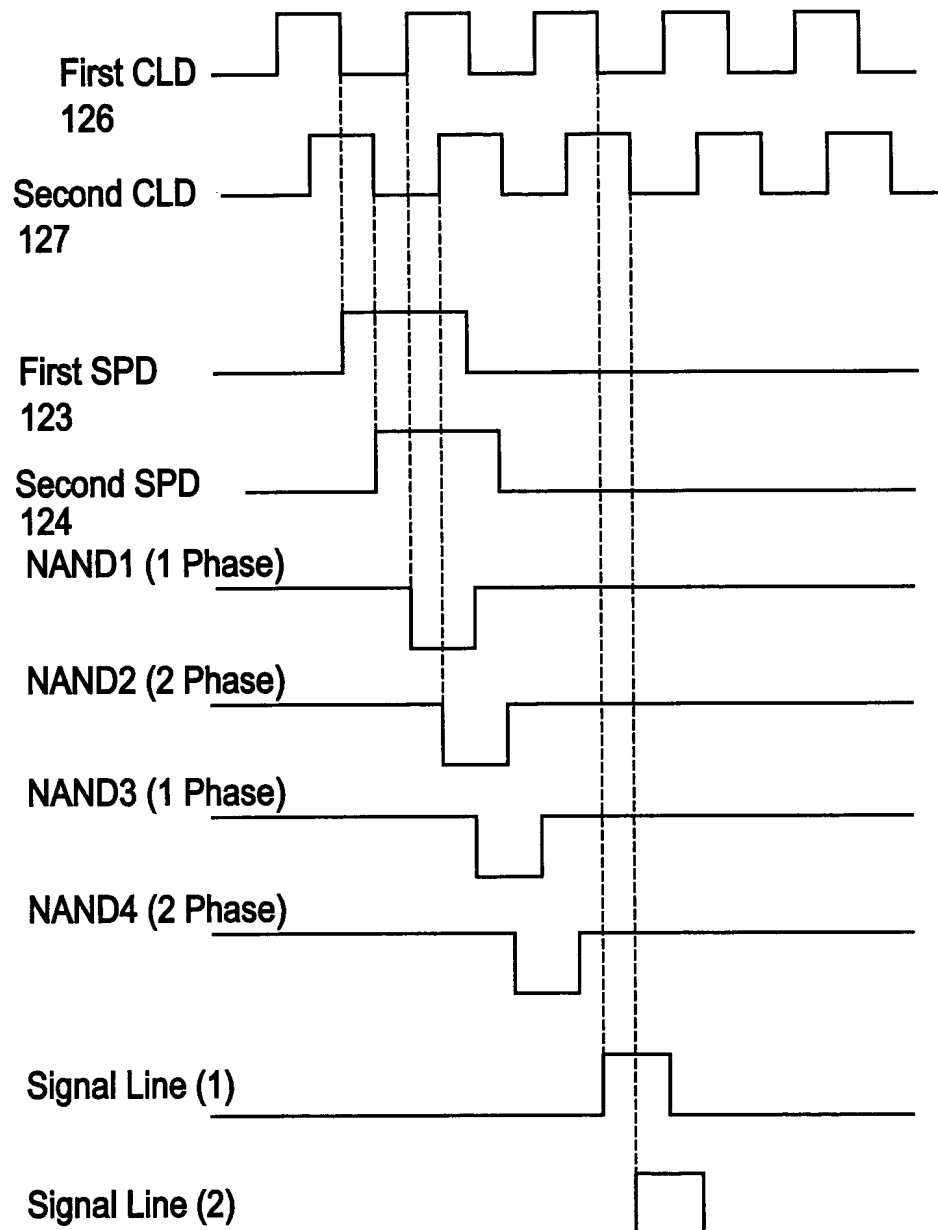
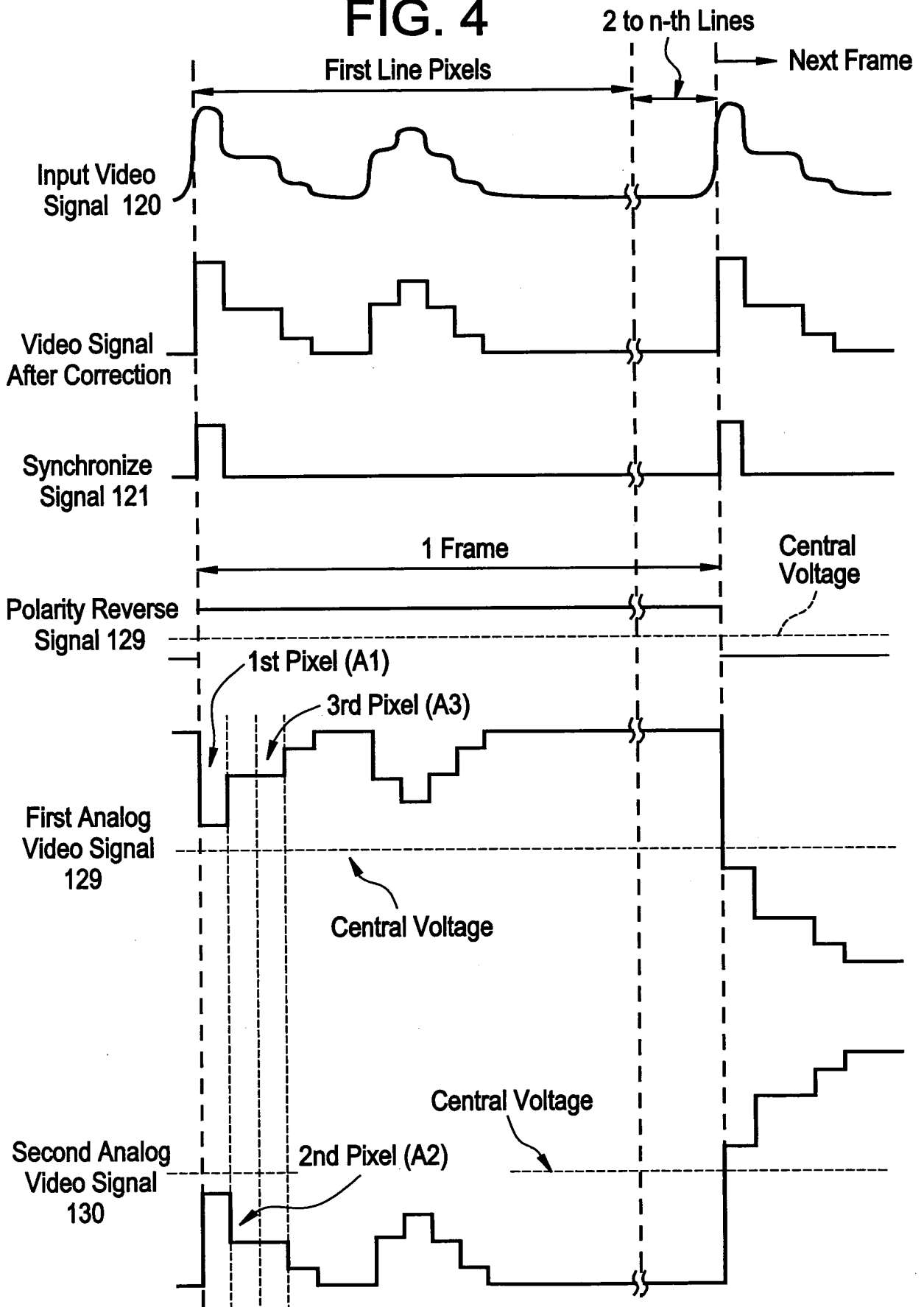
FIG. 3**Timing Chart of Source Driver Circuit**

FIG. 4

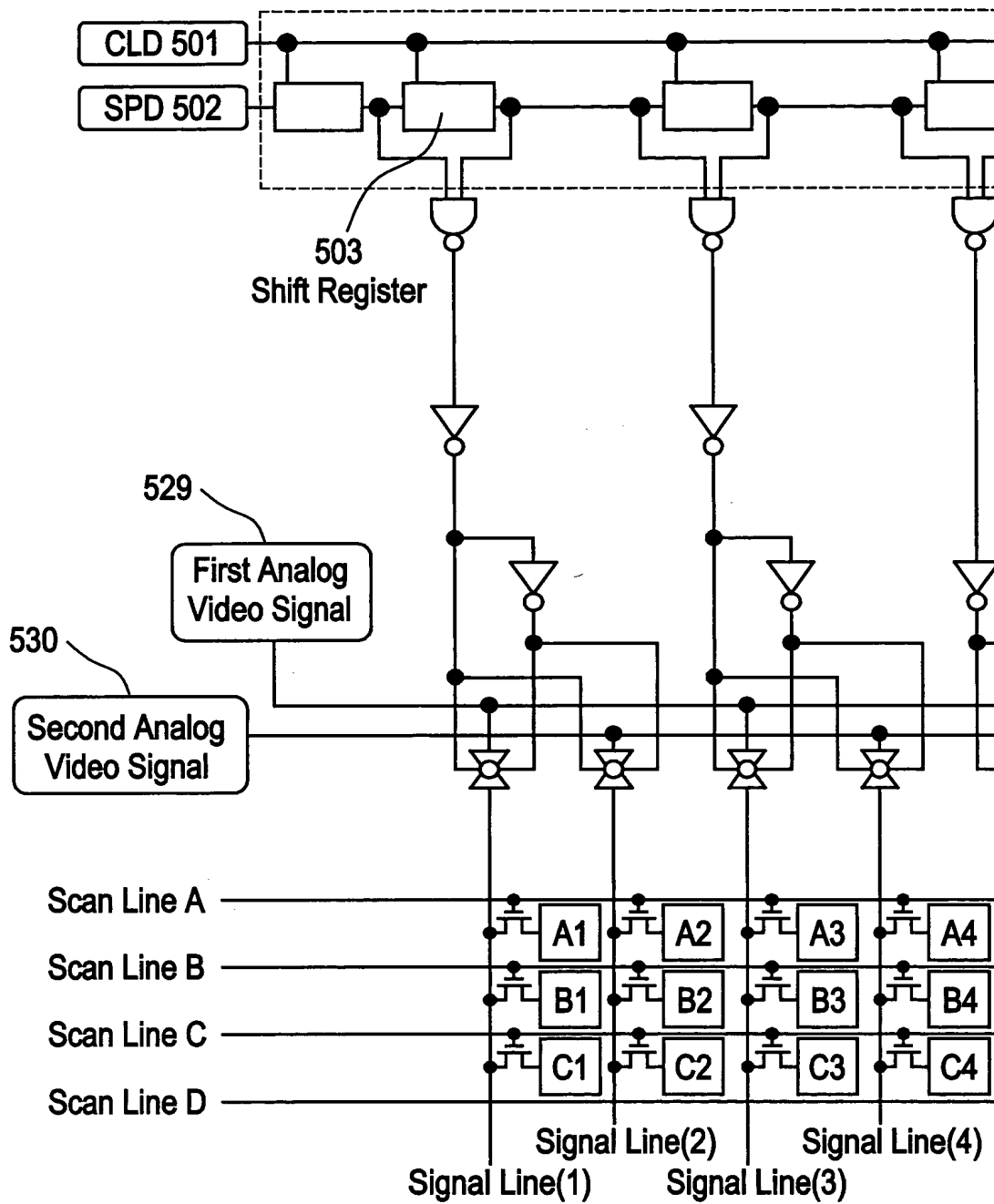


FIG.5B

Display Pattern

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4

FIG. 6

Rear Projection Type Display Device

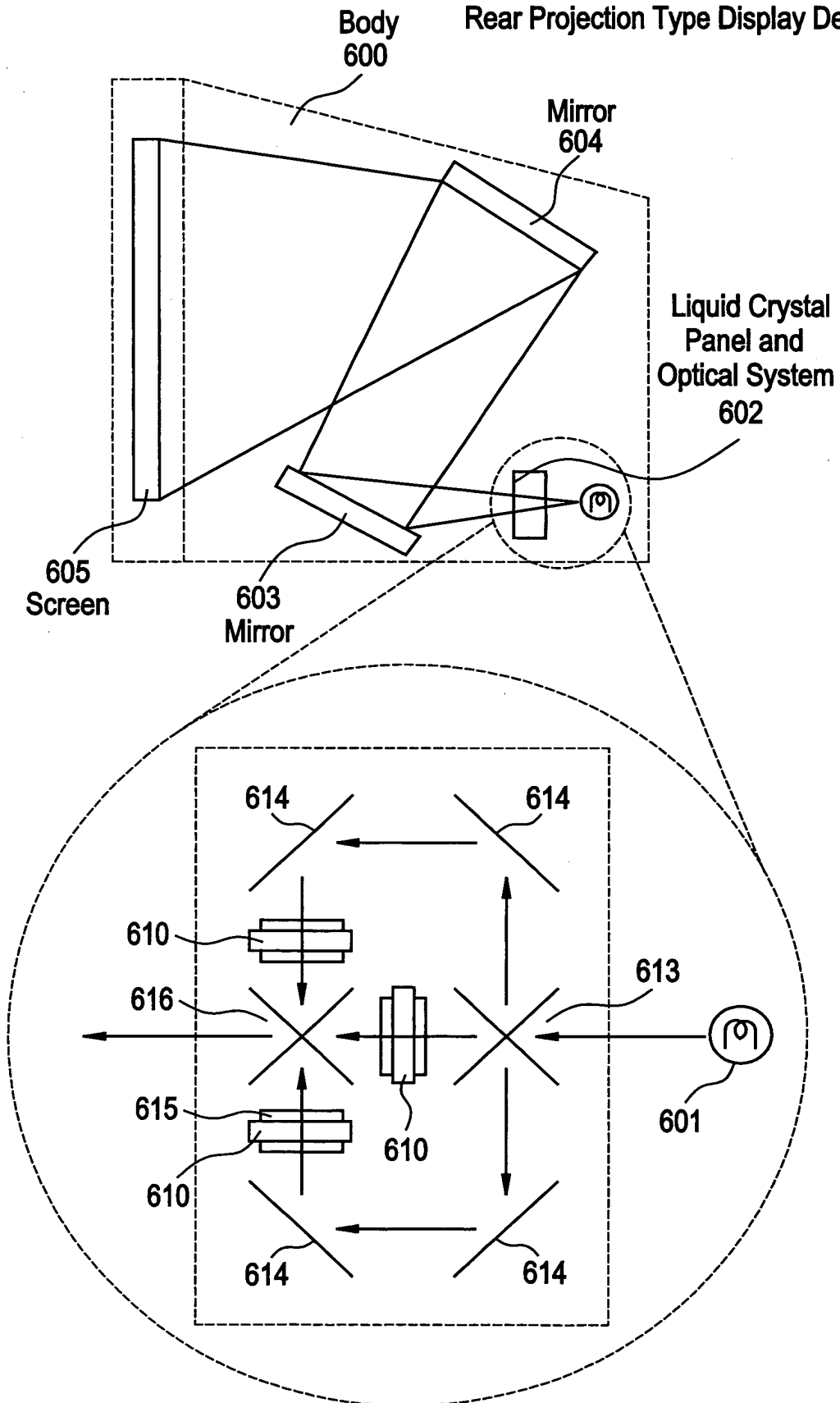


FIG. 7 PRIOR ART

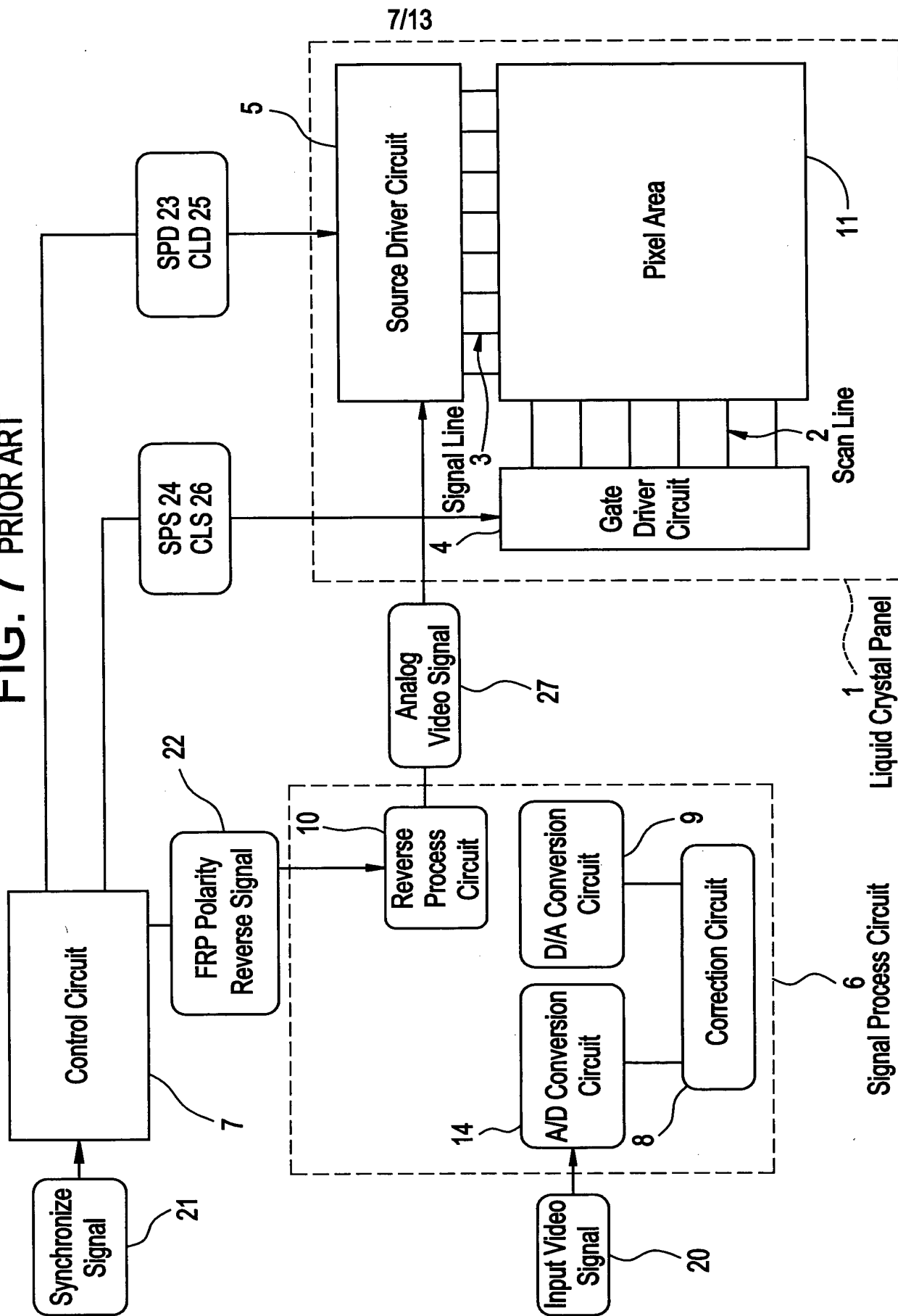


FIG. 8A

Circuit Diagram of Source Driver Circuit 5

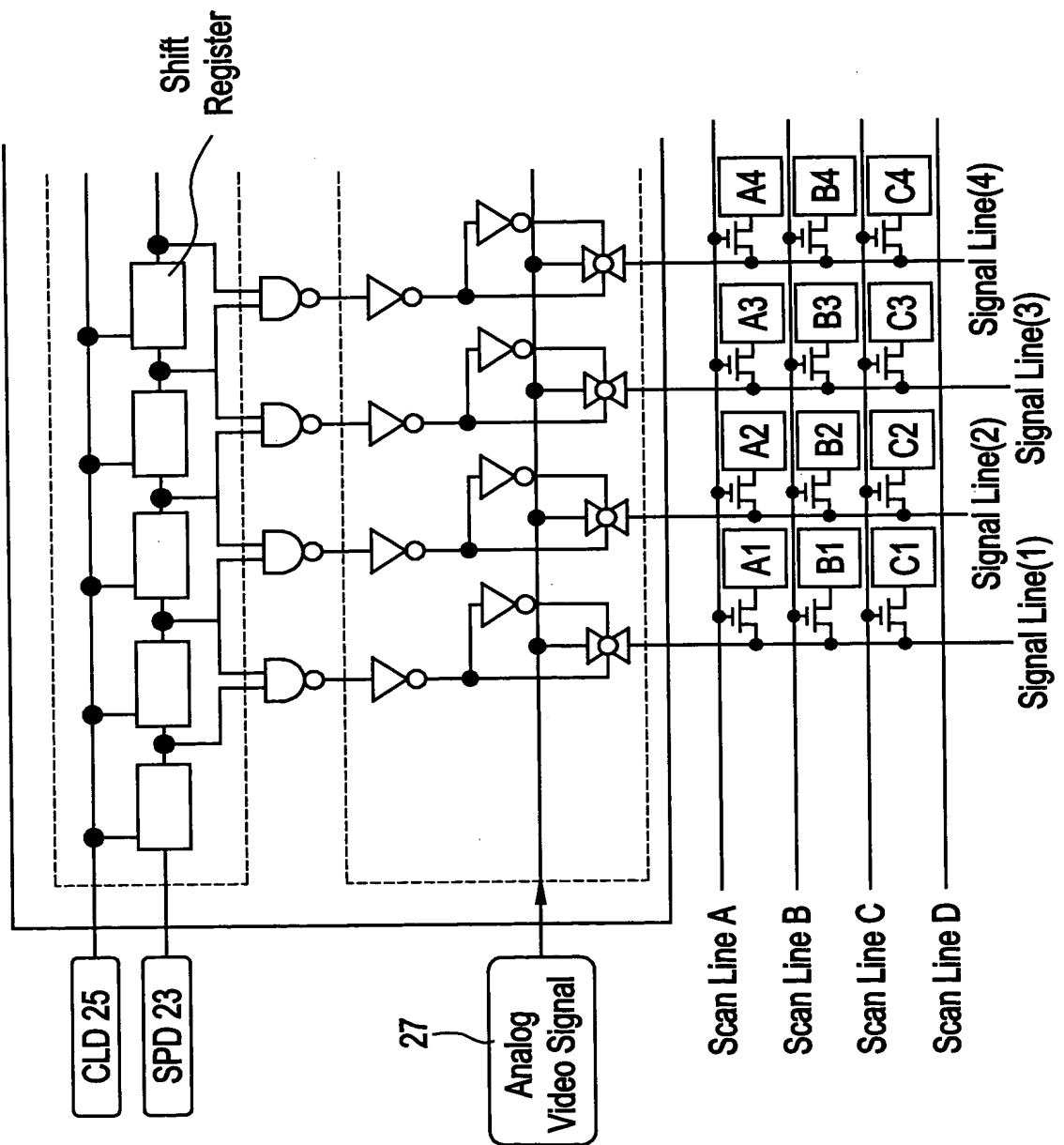


FIG. 8B

Display Pattern

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4

FIG. 9

Timing Chart of Source Driver Circuit

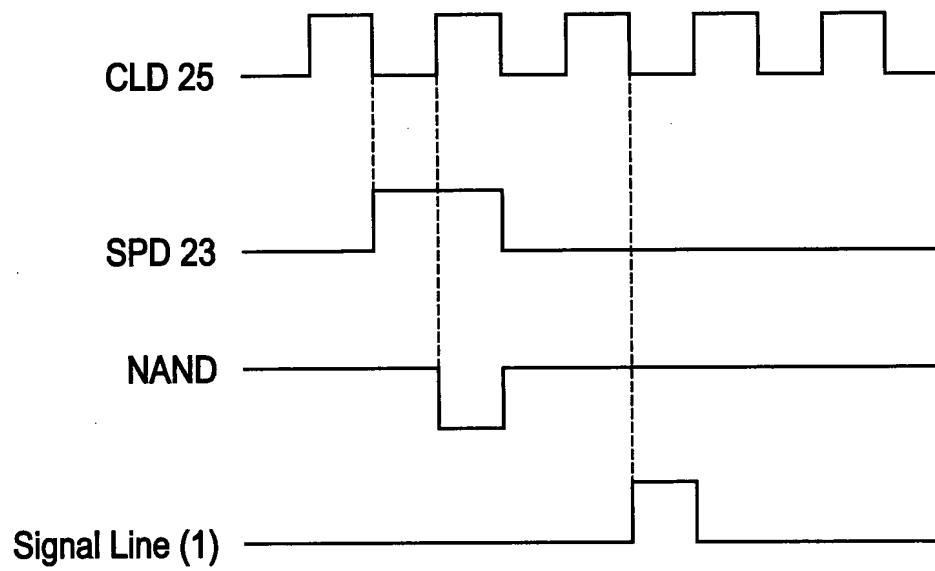
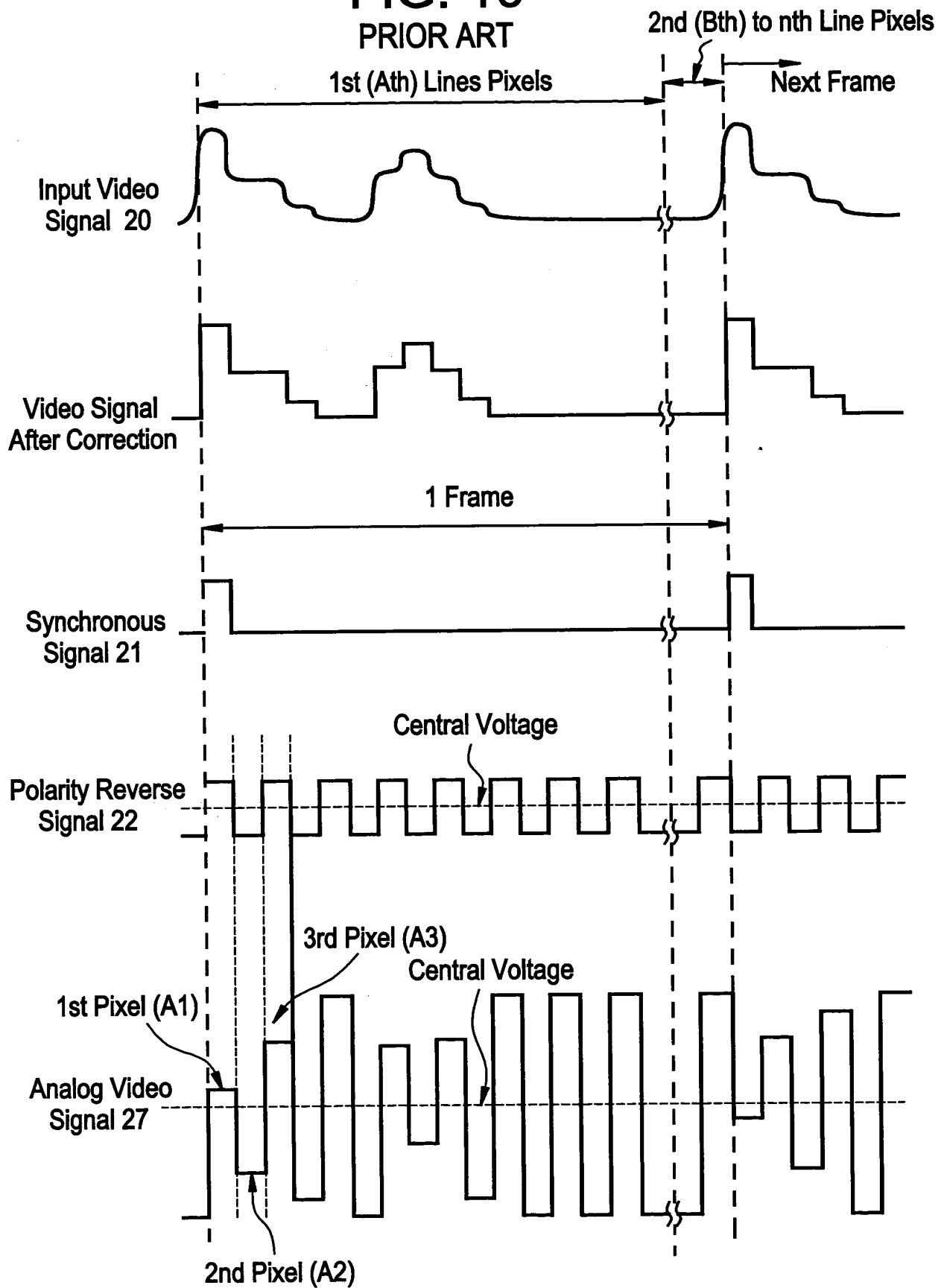


FIG. 10
PRIOR ART

A1	A2	A3	A4	A5	A6
B1	B2	B3	B4	B5	B6
C1	C2	C3	C4	C5	C6
D1	D2	D3	D4	D5	D6
E1	E2	E3	E4	E5	E6
F1	F2	F3	F4	F5	F6

FIG. 11B

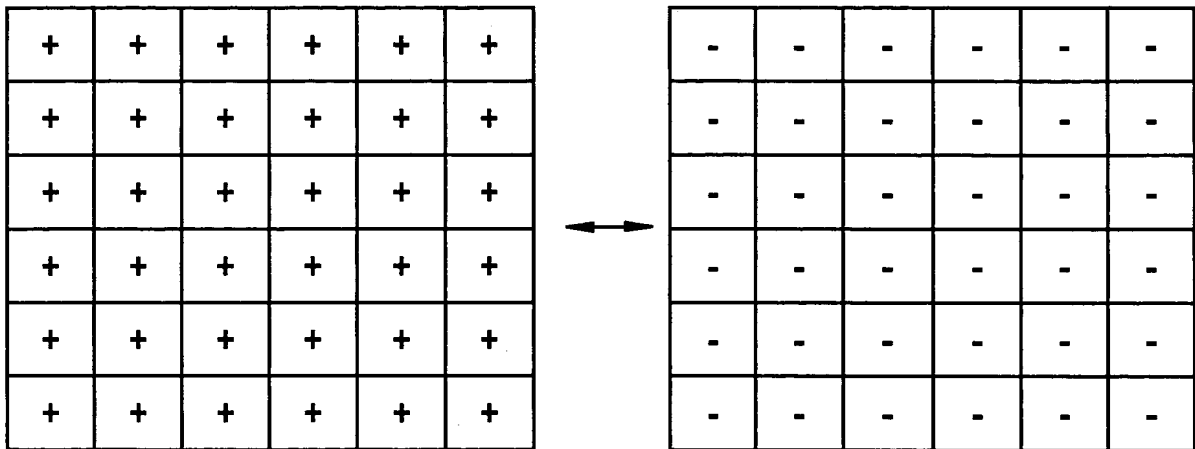
[illegible]

FIG. 11C

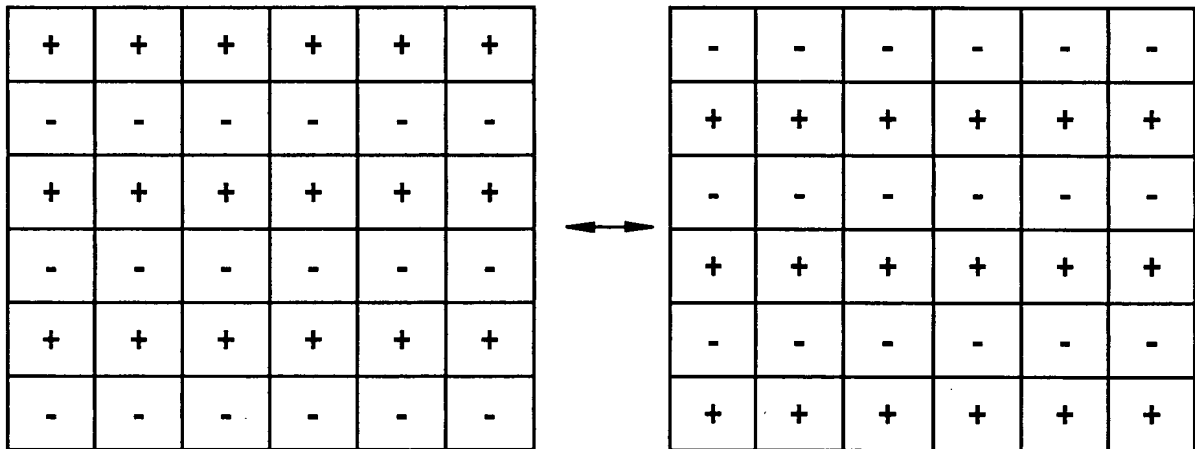
[illegible]

FIG. 12A

Display Pattern at Each Frame
Frame Inversion

**FIG. 12B**

Gate Line Inversion

**FIG. 12C**

Dot Inversion

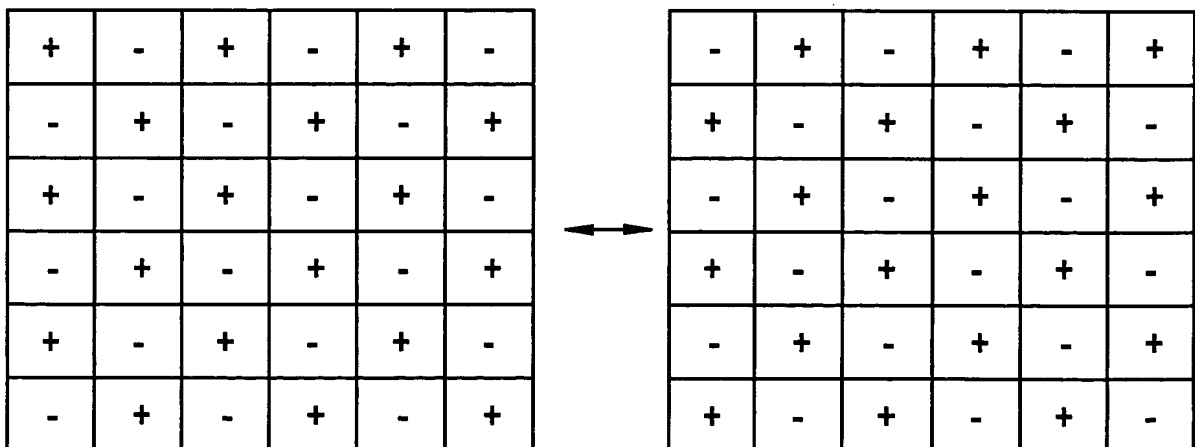


FIG. 13

